Amendments to the Specification

Please amend the abstract as indicated below:

Digital signal processing based methods and systems for receiving data signals include parallel receivers, multi-channel receivers, timing recovery schemes, and, without limitation, equalization schemes. The present invention is implemented as a multi-path parallel receiver in which an analog-to-digital converter ("ADC") and/or a digital signal processor ("DSP") are implemented with parallel paths that operate at lower rates than the received data signal. In an embodiment, a parallel DSP-based receiver in accordance with the invention includes a separate timing recovery loop for each ADC path. ~~The separate timing recovery loops can be used to compensate for timing phase errors in the clock generation circuit that are different for each path.~~ In an embodiment, a parallel DSP-based receiver includes a separate automatic gain control (AGC) loop for each ADC path. ~~The separate AGC loops can be used to compensate for gain errors on a path-by-path basis.~~ In an embodiment, a parallel DSP-based receiver includes a separate offset compensation loop for each ADC path. ~~The separate offset compensation loops can be used to independently compensate for offsets that are different for each path.~~ In an embodiment the present invention is implemented as a multi-channel receiver that receives a plurality of data signals. ~~In an embodiment, one or more of the following types of equalization are performed, alone and/or in various combinations with one another: Viterbi equalization; feed-forward equalization ("FFE"); and/or decision feed-back equalization ("DFE").~~